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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,737	08/19/2003	Fumiaki Karasawa	116884	3798

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EXAMINER	
PERKINS, PAMELA E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,737	KARASAWA ET AL.	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the application papers on 19 August 2003. Claims 1-57 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4-6, 11, 12, 14-16, 19, 20, 23-26, 28, 30, 36, 39, 41, 44, 46, 53, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi et al. (6,353,267) in view of Tomita et al. (5,874,365).

Ohuchi et al. disclose a method of manufacturing a semiconductor device where a protrusion (31) is formed on a semiconductor substrate (30) having a first area, the protrusion (31) protruding above the first area (Fig 3-B; col. 4, lines 4-13); disposing a resin layer (32) on a first area of a semiconductor substrate (30); disposing a through hole (35) overlapping the first area; and grinding the semiconductor substrate (30) from a surface opposite to the surface on which the protrusion (31) is formed (Fig. 4-B; col. 4, lines 25-44).

Although Ohuchi et al. does not specifically disclose having a first area and a second area surrounding the first area, it is inherent in circuit formation to a periphery are (second area) surround a circuit area (first area).

Ohuchi et al. do not disclose disposing a support on a surface of the semiconductor substrate on which the protrusion is formed, a part of the support overlapping with the second area being thicker than another part of the support overlapping with the first area.

Tomita et al. disclose a method of manufacturing a semiconductor device where a protrusion is formed on a semiconductor substrate (2) having a first area and a second area surrounding the first area, the protrusion protruding above the first area; disposing a resin layer (7) on a first area of the semiconductor substrate (2); and disposing a support (8) on a surface of the semiconductor substrate (2) on which the protrusion is formed, a part of the support (8) overlapping with the second area being thicker than another part of the support overlapping with the first area (col. 3, lines 1-12; col. 8, lines 4-8).

Since Ohuchi et al. and Tomita et al. are both from the same field of endeavor, a method of manufacturing a semiconductor device, the purpose disclosed by Tomita et al. would have been recognized in the pertinent art of Ohuchi et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ohuchi et al. by disposing a support on a surface of the semiconductor substrate on which the protrusion is formed, a part of the support overlapping with the second area being thicker than another part of the support overlapping with the first area as taught by Tomita et al to prevent scratching (col. 1, lines 56-65)

Referring to claims 4, 14 & 26, Tomita et al. disclose the second area being an outer end of the semiconductor substrate (2) (Fig, 1; col. 3, lines 1-12).

Referring to claims 5 & 28, Tomita et al. disclose the step of disposing the support (8) including forming the support (8) by coating the semiconductor substrate (2) with resin by spin-coating (col. 3, lines 41-51).

Referring to claim 6 & 30, Tomita et al. disclose the step of disposing the support (8) including forming a raised portion of the resin on the second area (col. 8, lines 4-9).

Referring to claim 15, Ohuchi et al. in view of Tomita et al. disclose the support being formed on the periphery of the through hole and has a step that disposes an outer end of the semiconductor substrate (Ohuchi: col. 4, lines 21-24; Tomita: col. 3, lines 1-12).

Referring to claims 16, 44 & 46, Tomita et al. disclose the support (8) being made of resin (col. 3, lines 41-60).

Referring to claims 19, 36, 39, 41, 53, 55 & 56, Ohuchi et al. disclose cutting the semiconductor substrate (30) after the step of grinding the semiconductor substrate (30) (Fig. 4-b, 4-D; col. 5, lines 1-4).

Referring to claim 20, Tomita et al. disclose removing the support (8) from the semiconductor substrate (2) after the step of etching/grinding the semiconductor substrate (2) (col. 7, lines 39-51).

Referring to claim 24, Ohuchi et al. disclose a circuit board equipped with the semiconductor device (col. 4, lines 45-54).

Claims 3, 7-10, 13, 17, 18, 27, 29, 31-35, 37, 38, 40, 42, 43, 45, 47-52, 54 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi et al. in view

of Tomita et al. as applied to claims 1, 2, 11, and 12 above, and further in view of Ogawa et al. (4,418,284).

Ohuchi et al. in view of Tomita et al. disclose the subject matter claimed above except disposing a protruding electrode on the resin layer.

Ogawa et al. disclose a method of manufacturing a semiconductor device where a protrusion (3, 4) is formed on a semiconductor substrate (1) having a first area and a second area surrounding the first area, the protrusion (3, 4) protruding above the first area (Fig. 4A); disposing a resin layer (13) on a first area of a semiconductor substrate (1) (Fig. 4B); and disposing a protruding electrode (12) on the resin layer (13) (Fig. 4C).

Since Ohuchi et al. and Ogawa et al. are both from the same field of endeavor, a method of manufacturing a semiconductor device, the purpose disclosed by Ogawa et al. would have been recognized in the pertinent art of Ohuchi et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ohuchi et al. by disposing a protruding electrode on the resin layer as taught by Ogawa et al. to prevent noise (col. 1, lines 6-15).

Referring to claims 7, 32 & 33, Ogawa et al. disclose pressing to planarize a surface of the resin (13) (col. 5, lines 4-40).

Referring to claims 8, 9 & 10, Ogawa et al. disclose an adhesive sheet having an adhesive layer (14) thicker than the height of the protrusion (3, 4); and pressing the semiconductor substrate (1) against the adhesive sheet to eject at least a part of the adhesive layer (14) outside the protrusion (3, 4) and resin layer (13) (Fig. 4D; col. 4, lines 33-66).

Referring to claims 17, 45 & 47, Ogawa et al. disclose curing the resin (13) (col. 4, line 61 thru col. 6, line 3).

Referring to claims 18, 21, 34, 35, 38, 40, 42 & 48-52, Ogawa et al. disclose the first area (111) being an area of an effective chip having an integrated circuit and becoming a product; and the second area (115) being an area of a periphery chip which does not become a product (Fig. 9; col. 8, lines 13-22).

Referring to claim 27, Tomita et al. disclose the second area being an outer end of the semiconductor substrate (2) (Fig, 1; col. 3, lines 1-12).

Referring to claim 29, Tomita et al. disclose the step of disposing the support (8) including forming the support (8) by coating the semiconductor substrate (2) with resin by spin-coating (col. 3, lines 41-51).

Referring to claim 31, Tomita et al. disclose the step of disposing the support (8) including forming a raised portion of the resin on the second area (col. 8, lines 4-9).

Referring to claims 37, 43, 54 & 57, Ohuchi et al. disclose cutting the semiconductor substrate (30) after the step of grinding the semiconductor substrate (30) (Fig. 4-b, 4-D; col. 5, lines 1-4).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi et al. in view of Ogawa et al.

Ohuchi et al. disclose the subject matter claimed above except disposing a protruding electrode on the resin layer.

Ogawa et al. disclose a method of manufacturing a semiconductor device where a protrusion (3, 4) is formed on a semiconductor substrate (1) having a first area and a second area surrounding the first area, the protrusion (3, 4) protruding above the first area (Fig. 4A); disposing a resin layer (13) on a first area of a semiconductor substrate (1) (Fig. 4B); and disposing a protruding electrode (12) on the resin layer (13) (Fig. 4C).

Since Ohuchi et al. and Ogawa et al. are both from the same field of endeavor, a method of manufacturing a semiconductor device, the purpose disclosed by Ogawa et al. would have been recognized in the pertinent art of Ohuchi et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ohuchi et al. by disposing a protruding electrode on the resin layer as taught by Ogawa et al. to prevent noise (col. 1, lines 6-15).

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi et al. in view of Ogawa et al. as applied to claim 21 above, and further in view of Takeuchi et al. (6,005,474).

Ohuchi et al. in view of Ogawa et al. disclose the subject matter claimed above except the second area including an area of a part which includes a side face of the semiconductor substrate and becomes a semiconductor chip.

Takeuchi et al. disclose a method of manufacturing a semiconductor device where a protrusion (11) is formed on a semiconductor substrate (1) having a first area and a second area surrounding the first area, the protrusion (11) protruding above the first area; and disposing a resin layer (15) on a first area of a semiconductor substrate

(1) (col. 6, lines 39-67). Takeuchi et al. further disclose the second area including an area of a part which includes a side face of the semiconductor substrate (1) and becomes a semiconductor chip (Fig. 2; col. 7, lines 1-19).

Since Ohuchi et al. and Takeuchi et al. are both from the same field of endeavor, a method of manufacturing a semiconductor device, the purpose disclosed by Takeuchi et al. would have been recognized in the pertinent art of Ohuchi et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ohuchi et al. by the second area including an area of a part which includes a side face of the semiconductor substrate and becomes a semiconductor chip as taught by Takeuchi et al. to prevent breakage (col. 7, lines 11-56).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nakaiyo et al. (6,420,213) disclose a method of manufacturing a semiconductor device where a protrusion is formed on a semiconductor substrate having a first area and a second area surrounding the first area, the protrusion protruding above the first area; disposing a resin layer on a first area of a semiconductor substrate; and pressing to planarize a surface of the resin.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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